REMARKS/ARGUMENTS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-8, and 17-20 are pending in this case. Claims 1 and 17 are amended herein and claims 19-20 are added herein.

The Examiner rejected claims 1-3, 6, 7, 17 and 18 under 35 U.S.C. § 102(e) as being anticipated by Saia et al. (U.S. Patent No. 5,874,770).

Applicant respectfully submits that claim 1 is unanticipated by Saia et al as there is no disclosure or suggestion in Saia of a thin film resistor embedded within a multi-level dielectric layer between a lower metal interconnect layer and an upper metal interconnect layer, wherein the thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer. Saia teaches a flexible interconnect film which includes a number of interconnect layers 21, 22, and those connected to 56, 52, etc. The resistor 28 is in direct contact with interconnect 21. Interconnect 21 is located directly on a portion of resistor layer 28 and accordingly is not physically separated in a vertical direction from resistor layer 28. In contrast, the claim requires that the resistor layer is physically separated, in its entirety, in a vertical direction from any metal interconnect layer. The claimed resistor is located between metal interconnect layers instead of at an interconnect layer, such as interconnect 21 and thus has the advantage of increased flexibility in designing the resistor since processes, materials, and chemicals do not have to satisfy the conditions of both the resistor and an interconnect layer. This is not disclosed or suggested by Saia. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Saia et al.

Applicant respectfully submits that claim 17 is unanticipated by Saia as there is no disclosure or suggestion of the claimed thin film resistor in a semiconductor chip of an IC. Saia teaches a flexible interconnect film to which circuit chips 44 may be attached. Saia does not disclose or suggest a thin film resistor 28 as part of a semiconductor chip but rather as a part external to the circuit chip 44. Accordingly, Applicant respectfully submits that claims 17 and 18 are unanticipated by Saia.

The Examiner rejected claims 4, 5 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Saia et al. as applied to claim 1, and further in view of Linn et al. (U.S. Patent No. 5,547,896).

Applicant respectfully submits that claims 4, 5, and 8 are patentable over Saia in view of Linn for the same reasons discussed above relative to claim 1 from which these claims depend.

Applicant respectfully submits that newly added claim 19 is patentable over the references as there is no disclosure or suggestion in the references of a first and a second metal interconnect layer, wherein there are no additional metal interconnect layers between the first and second metal interconnect layers, a multi-level dielectric layer located between the first and second metal interconnect layers, and a thin film resistor embedded within the multi-level dielectric layer such that the multi-level dielectric layer separates the thin film resistor from both the first metal interconnect layer and the second metal interconnect layer. Interconnect layers 46 and 47 do not satisfy the claim requirement of first and second metal interconnect layer because there are addition metal interconnect layers between them (i.e., metal interconnects 21 and 22). Accordingly, Applicant respectfully submits that claim 19 and the claim dependent theroen are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-8 and 17-20. If the Examiner has any questions or

other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated

Jacqueline J. Garner
Reg. No. 36,144
Phone: (214) 532-9348
Fax: (972) 917-4418